What Is Claimed Is:

1. A shift-register unit, comprising:

a first transistor having a first source/drain coupled to a first terminal, a second source/drain, and a first gate coupled to a reset signal to stop the shift-register unit outputting a pulse signal;

a second transistor having a third source/drain coupled to the second source/drain, a fourth source/drain coupled to a second terminal, and a second gate coupled to a setting signal to the initial shift-register unit;

a third transistor having a fifth source/drain coupled to an output terminal, a third gate coupled to the second source/drain and a sixth source/drain coupled to a clock signal to start outputting the pulse signal; and

a fourth transistor having a seventh source/drain coupled to the first terminal, an eighth source/drain coupled to the output terminal and a fourth gate coupled to a refresh signal to set a voltage level of the shift-register unit in a standby mode.

2. The shift-register unit as claimed in claim 1, further comprising a fifth transistor having a ninth source/drain coupled to the first terminal, a tenth source/drain coupled to the second source/drain and a fifth gate coupled to a preset signal to set a voltage level of the third gate.

3. The shift-register unit as claimed in claim 2, wherein the transistors are p-type transistors and the first terminal

is coupled to a power source and the second terminal is coupled to the setting signal.

4. The shift-register unit as claimed in claim 2, wherein the transistors are p-type transistors and the voltage level of the first terminal exceeds that of the second terminal.

5. The shift-register unit as claimed in claim 2, wherein the transistors are n-type transistors and the first terminal is coupled to a ground level and the second terminal is coupled to the setting signal.

6. The shift-register unit as claimed in claim 2, wherein the transistors are n-type transistors and the voltage level of the second terminal exceeds that of the first terminal.

7. The shift-register unit as claimed in claim 1, wherein the transistors are thin film transistors.

8. The shift-register unit as claimed in claim 1, wherein the transistors are MOS transistors.

9. A shift-register circuit, comprising:

a first-stage shift-register unit, a final-stage shift-register unit and a plurality of middle-stage shift-register units connected between the first-stage shift-register unit and the final-stage shift-register unit, wherein the shift-register units are connected in serial and each shift-register unit outputs a pulse signal in sequence after the first-stage shift-register unit receives an initial setting signal;

each shift-register unit comprising:

a clock terminal for receiving a clock signal;

a setting terminal for receiving a setting signal for trigging the shift-register unit to output the clock signal as the pulse signal; and

a reset terminal for receiving a reset signal to reset the shift-register unit to stop outputting the pulse signal, wherein the reset terminals of the first-stage and the middle-stage shift-register units are respectively connected to the output signal of the subsequent stage shift-register unit, the reset terminal of the final-stage shift-register unit is connected to the output signal of the first-stage shift-register unit, the setting terminal of the middle-stage and the final-stage shift-register units are respectively connected to the output signal of the previous stage shift-register unit, the setting terminal of the first-stage shift-register unit is connected to the initial setting signal, the clock terminals of the odd stage shift-register units are connected to a first clock signal as the clock signal and the clock terminals of the even stage shift-register units are connected to a second clock signal as the clock signal.

10. The shift-register circuit as claimed in claim 9, wherein the shift-register unit comprises:

a first transistor having a first source/drain coupled to a first terminal, a second source/drain, and a first gate coupled to the reset terminal;

a second transistor having a third source/drain coupled to the second source/drain, a fourth source/drain coupled to a second terminal, and a second gate as the setting terminal; and

a third transistor having a fifth source/drain coupled to an output terminal, a third gate coupled to the second source/drain and a sixth source/drain as the clock terminal.

11. The shift-register circuit as claimed in claim 10, wherein the shift-register unit further comprises:

a fourth transistor having a seventh source/drain coupled to the first terminal, an eighth source/drain coupled to the output terminal and a fourth gate as a refresh terminal coupled to a refresh signal to set a voltage level of the shift-register unit in a standby mode; and

a fifth transistor having a ninth source/drain coupled to the first terminal, a tenth source/drain coupled to the second source/drain and a fifth gate as a preset terminal to set a voltage level of the third gate, wherein the refresh terminals of the even stage shift-register units are coupled to the first clock signal, and the refresh terminals of the odd stage shift-register units are coupled to the second clock signal.

12. The shift-register circuit as claimed in claim 11, wherein the first and the second clock signals have the same frequency and different duty cycles.

13. The shift-register circuit as claimed in claim 12, wherein the transistors are p-type transistors and the first terminal is coupled to a power source and the second terminal is coupled to the setting signal.

14. The shift-register unit as claimed in claim 12, wherein the transistors are p-type transistors and the voltage level of the first terminal exceeds that of the second terminal.

15. The shift-register unit as claimed in claim 12, wherein the transistors are n-type transistors and the first terminal is coupled to a ground level and the second terminal is coupled to the setting signal.

16. The shift-register unit as claimed in claim 12, wherein the transistors are n-type transistors and the voltage level of the second terminal exceeds that of the first terminal.

17. The shift-register unit as claimed in claim 10, wherein the transistors are thin film transistors.

18. The shift-register unit as claimed in claim 10, wherein the transistors are MOS transistors.

19. A shift-register circuit, comprising:

a first-stage shift-register unit, a second-stage shift-register unit, a third-stage shift-register unit and a fourth-stage shift-register unit

connected in serial, wherein each shift-register unit outputs a pulse signal in sequence after the first-stage shift-register unit receives an initial setting signal;

each shift-register unit comprising:

a clock terminal for receiving a clock signal;

a setting terminal for receiving a setting signal for triggering the shift-register unit to output the clock signal as the pulse signal; and

a reset terminal for receiving a reset signal to reset the shift-register unit to stop outputting the pulse signal, wherein the reset terminals of the first-stage, the second-stage and the third-stage shift-register units are respectively connected to the output signal of the subsequent stage shift-register unit, the setting terminal of the second-stage, the third-stage and the fourth stage shift-register units are respectively connected to the output signal of the previous stage shift-register unit, the setting terminal of the first-stage shift-register unit is connected to the initial setting signal, the clock terminals of the first-stage and the fourth-stage shift-register units are connected to a first clock signal as the clock signal, the clock terminal of the second-stage shift-register unit is connected to a second clock signal as the clock signal and the clock terminal of the third-stage shift-register

unit is connected to a third clock signal as the clock signal.

20. The shift-register circuit as claimed in claim 19, wherein the shift-register unit comprises:

a first transistor having a first source/drain coupled to a first terminal, a second source/drain, and a first gate coupled to the reset terminal;

a second transistor having a third source/drain coupled to the second source/drain, a fourth source/drain coupled to a second terminal, and a second gate as the setting terminal; and

a third transistor having a fifth source/drain coupled to an output terminal, a third gate coupled to the second source/drain and a sixth source/drain as the clock terminal.

21. The shift-register circuit as claimed in claim 20, wherein the shift-register unit further comprises:

a fourth transistor having a seventh source/drain coupled to the first terminal, an eighth source/drain coupled to the output terminal and a fourth gate as a refresh terminal coupled to a refresh signal to set a voltage level of the shift-register unit in a standby mode; and

a fifth transistor having a ninth source/drain coupled to the first terminal, a tenth source/drain coupled to the second source/drain and a fifth gate as a preset terminal to set a voltage level of the third gate, wherein the refresh terminal of the first-stage

shift-register unit is coupled to the first clock signal, the refresh terminal of the second-stage shift-register unit is coupled to the second clock signal and the refresh terminal of the third-stage shift-register unit is coupled to the third clock signal.

22. The shift-register circuit as claimed in claim 21, wherein the first, the second and the third clock signals have the same frequency and different duty cycles.

23. The shift-register circuit as claimed in claim 22, wherein the transistors are p-type transistors and the first terminal is coupled to a power source and the second terminal is coupled to the setting signal.

24. The shift-register unit as claimed in claim 22, wherein the transistors are p-type transistors and the voltage level of the first terminal exceeds that of the second terminal.

25. The shift-register unit as claimed in claim 22, wherein the transistors are n-type transistors and the first terminal is coupled to a ground level and the second terminal is coupled to the setting signal.

26. The shift-register unit as claimed in claim 22, wherein the transistors are n-type transistors and the voltage level of the second terminal exceeds that of the first terminal.

27. The shift-register unit as claimed in claim 20, wherein the transistors are thin film transistors.

28. The shift-register unit as claimed in claim 20, wherein the transistors are MOS transistors.